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Focal Plane Compression Sensors Based On Pixel Parallel and Column Parallel Architectures

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Abstract

We propose a novel integration of compression and sensing in order to enhance performance of the image sensor. By integrating compression function on the sensor plane, the image signal that has to be readout from the sensor is significantly reduced. Thus, the integration can consequently increase the pixel rate of the sensor.

The compression scheme we make use of is conditional replenishment that detects and encodes moving areas. In this paper, we discuss design and implementation of two architectures for focal plane compression. One is pixel parallel approach and the other is column parallel approach. We describe and compare both approaches. We show some results obtained by implementation of the pixel parallel approach.

1 Introduction

An imaging sensor corresponds to the retina in biological vision. The retina not only detects image signals but also processes limited low-level tasks including compression in order to enhance imaging performance and to preprocess tasks for later stages [1]. Then, from the point of view of biological vision, integration of processing and sensing is reasonable in order to augment sensing performance. Compression seems one of the most desirable processing for the sensor.

In this paper, we investigate a novel integration of image sensor and image compression. We present novel image sensors which compress image signal on the sensor plane. By the integration of sensing and compression, the image signal that has to be readout from the sensor can be significantly reduced, and the integration can consequently increase the pixel rate of the sensor because the high bandwidth is the fundamental limitation to the feasibility of high pixel rate imaging such as high frame rate imaging and high resolution imaging. The aim of compression on sensor is to augment the performance of the sensor, and it is different from that of digital compression.

Related works in terms of integration of signal processing and sensing are found in those areas of machine vision applications and neural network researches[2, 3]. Those works are referred to as smart sensors, vision chips or computational sensors. By integrating sensing and processing, the parallel nature of the image signal can be exploited and the processing gets remarkably faster. In those works, for example, a silicon retina that is a device which computes spatial derivatives of an image and an analog network that calculates optical flow have been developed. Most of those works are focused on how to execute early-vision processing in analog domain. Most computational sensors are fabricated by CMOS technology.

As for imaging devices, CCDs have been dominating so far. However, different from CCDs, CMOS compatible image sensor technology is attracting attention. (The CMOS compatible image sensor is called CMOS sensor or active pixel sensor.) It has one or more active transistors in a pixel[5, 6, 7]. From the application point of view, one of the major advantages of CMOS sensor is that it is suitable to integration with CMOS circuits that enables on-chip processing, while integration with CMOS circuits is not easy for CCDs. So far, signal processing such as AD conversion has been integrated on chip[8]. The other advantages are that it provides random access capability, do not need charge transfer, has high sensitivity and allow large arrays etc [6].

Our proposed sensor is a CMOS-based computational image sensor which compresses image signal on the sensor plane. In this paper, we present our approaches to a novel integration of image sensing and compression. We describe two architectures; a pixel parallel approach and a column parallel approach. We present the designs of the architectures and some results obtained so far. (Among the two,

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we have presented the first prototype of the pixel parallel approach in [9], but we present in this paper a new complete design.)

2 Image Compression

Our proposed compression sensor utilizes a conditional replenishment algorithm. It detects temporally changing pixels as active pixels and output them. The algorithm was originally proposed for easily-implementable digital compression method [4], but now we make use of it in a different way.

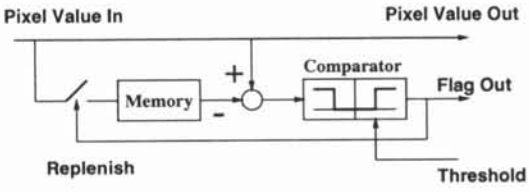

Figure 1: Description of coding algorithm in each pixel by conditional replenishment

Figure 1 illustrates the scheme of conditional replenishment. Current pixel values are compared to those of the last replenished value stored in the memory, and the values and addresses of the pixels, for which the magnitudes of the difference is greater than the threshold, are extracted and coded. Although conditional replenishment is rather simple, it can achieve 10:1 compression ratio without significant degradation.

3 Design of On Sensor Compression Chips

The compression sensor needs, on the sensor plane, transducer and computational elements that are comparator and memory. There are various ways to implement the compression scheme. We investigate two approaches for the integration. One is a pixel parallel approach and the other is a column parallel approach. In the former method, each pixel has computational elements, and in the latter method each column has computational elements and the pixels in a column share comparators. Figure 2 illustrates both architectures.

3.1 Pixel Parallel Architecture

In the pixel parallel approach, each pixel has a transducer and computational elements, and each pixel individually detects changes and activates a flag signal if the difference between the current pixel vaule and the stored value exceeds a threshold. Then, it is able to make full use of two dimensional nature of image signals. We designed an analog circuit for the processing of each pixel, and circuits to control readout.

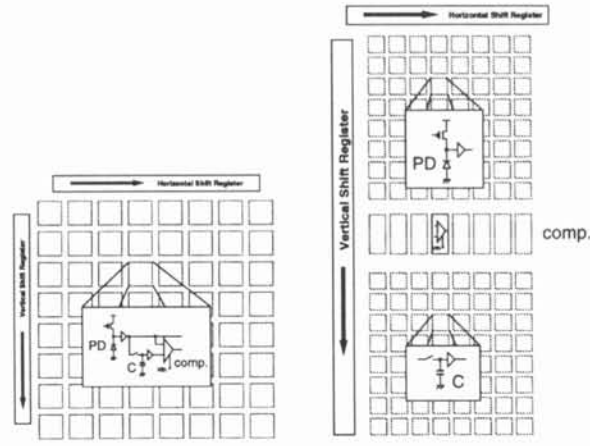

Figure 2: Illustrations of pixel parallel architecture (left) and column parallel architecture (right)

Fig. 3 shows a circuit contained in each pixel. Signal charge is sampled and held at C_1 and it is compared to the last replenished value stored in C_2 by a differential amplifier. Flag signal is activated when the sampled value in C_1 and the stored value in C_2 are unbalanced. The sensor sends out values of the pixels whose flag signals are activated. It is notable that the pixel value read out from the sensor is not processed at all.

Fig. 4 shows the design of the entire sensor array. Using horizontal and vertical shift registers, the sensor selects a pixel and read it out. As shown in the figure, it has two horizontal shift registers. One of them scans pixels in a smart way; it is controlled by the flag signals, and it skips non-activated pixels and selects only activated pixels so that the output sequence is compact and does not have blank spaces. The design of the circuit of this smart shift register is shown in Fig. 5.

The flag signals are also used for rate control. The flag signals are summed up in analog domain and the threshold is adjusted so that the number of the readout pixels can be constant.

The disadvantage of the pixel parallel approach is the fill factor. Because of the circuit (34 transistors) in the pixel, it is not able to have high fill factor unless an advanced structure such as a layered structure is available. The current design has 22μm $\times$ 22μm PD area in 160μm $\times$ 160μm pixel area under 2μm geometric rule.

3.2 Prototype Chip

Based on the pixel parallel approach, we have fabricated prototype sensors. Figure 7 shows a new prototype chip based on the new design described above. It has 32 pixels $\times$ 32 pixels. Different from our previous prototype[9], the sensor has complete compression functions. It has active flag counter for rate control, and smart scanning horizontal shift register. Furthermore, the circuit in each pixel is re-designed so that its power consumption is much

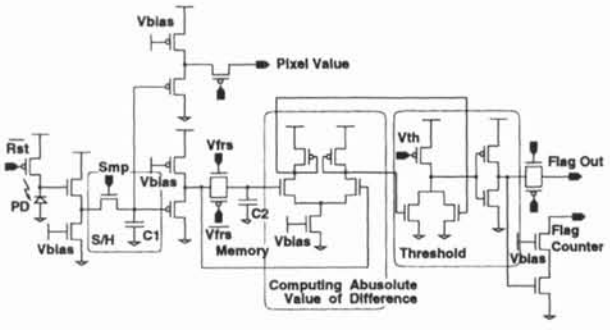

Figure 3: Design of the processing circuit in a pixel.

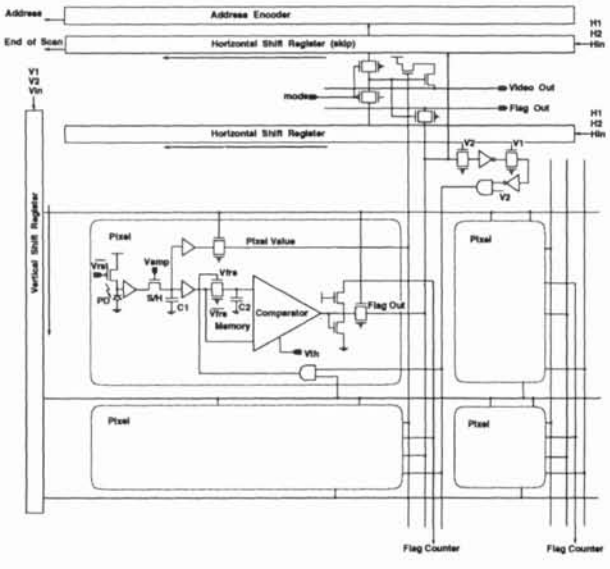

Figure 4: Design of on sensor compression chip by pixel parallel architecture.

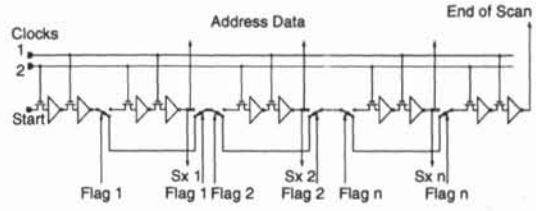

Figure 5: Smart shift register controlled by activated pixels

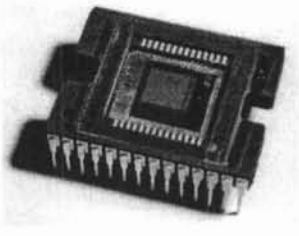

Figure 6: A new prototype chip of the on-sensor-compression

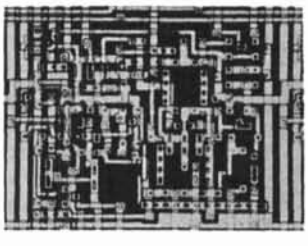

Figure 7: A single pixel of the prototype sensor

lowered.

Figure 8 shows an image obtained by the prototype sensor. In the experiments, an image of "T" is projected onto the sensor. The flag outputs when the image is moved or switched are also shown in fig. 8. It is verified that the sensor detects incident light and the processing circuit of the pixel properly works. When the incident light turned on and off, the entire figure of "T" activates flags. When "T" moves horizontally or vertically, vertical or horizontal edges of "T" activates flags.

The operation speed can be very high. At present, it is examined that the sensor can output image and flag signals at 1200 frames/second.

3.3 Column Parallel Architecture

In the design of the column parallel architecture, we separate transducer, comparator and memory elements. Figure 9 shows the outline of the architecture. By using this architecture, we can separate from the pixel all the transistors required for processing; each pixel contains transducer and 3 transistors. Thus, the fill factor can be improved and comparable to the orthodox CMOS sensors. Instead, it sacrifices the processing speed compared to the pixel parallel approach, because it processes image signal row by row. A prototype chip is under fabrication by 1.0 μm CMOS process.

4 Conclusion

We present a novel integration of sensing and compression and present two architectures for on sensor compression. We show the prototype based on the latest design and we will present detailed results obtained by the prototype.

Acknowledgment

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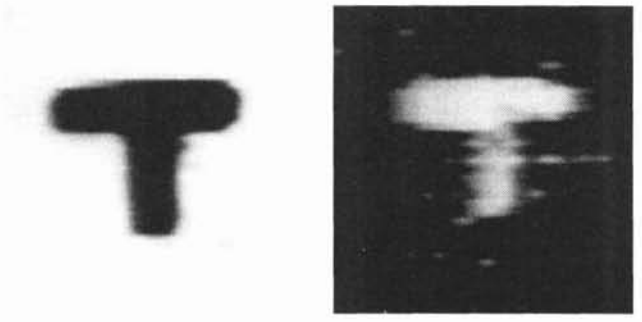
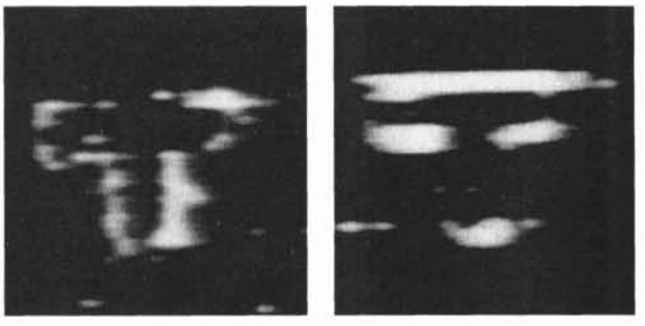


(a) An image output from the compression sensor

(b) Flag signal activated when the projected image "T" is switched on and off.



(c) Flag signal when the projected image "T" is moved horizontally.

(d) Flag signal when the projected image "T" is moved vertically.

Figure 8: Images obtained by the prototype sensor

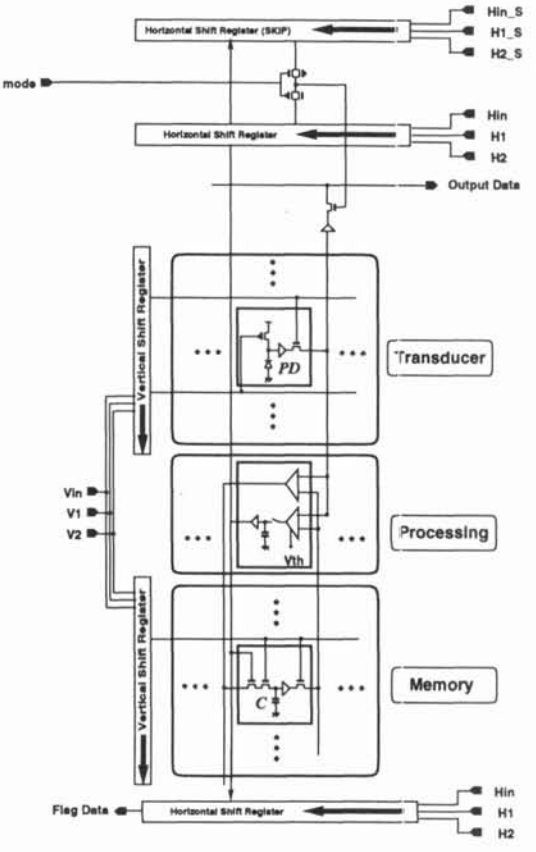


Figure 9: A description of the design of column parallel architecture

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