A REAL-TIME VISION SYSTEM USING INTEGRATED MEMORY ARRAY PROCESSOR PROTOTYPE LSI

Yoshihiro Fujita, Nobuyuki Yamashita, Shin'ichiro Okazaki

C&C Information Technology Research Laboratory
NEC Corporation
4-1-1 Miyazaki, Miyamae, Kawasaki, Kanagawa 216, Japan

ABSTRACT

This study reports on the performance of a Real-Time Vision System (RVS) and its use of an IMAP prototype LSI. This LSI integrates eight 8 bit processors and a 144 Kbit SRAM on a single chip. Processors operate in SIMD at 200 MIPS (25 MHz). The RVS was developed using 64 IMAP prototype LSIs connected in series in a 512 processor system configuration. Memory on the IMAP prototype LSI can be easily accessed from a host workstation through a VME bus. RVS performance is shown in real-time road-image processing and in a neural network simulation, as well as in low level image processing algorithms, such as filtering, histograms, Discrete Cosine Transform, and rotation. The RVS image processing is shown to be much faster than the video rate.

INTRODUCTION

Many image processing algorithms can be greatly expedited with SIMD processors [1][2]. In a previous study, the authors proposed an Integrated Memory Array Processor (IMAP) LSI, which integrates a large capacity memory and a one dimensional SIMD processor on a single chip to achieve a compact, high performance real-time vision system [3][4]. Since all processors can access their own individual part of the memory separately on the same chip, IMAP processors do not suffer from memory access bottleneck.

Figure 1 shows typical IMAP configuration, in which here an 8 Mbit memory, which has the same interface as a VRAM, is integrated with 128 8 bit processors. The IMAP holds images on the chip and performs high speed image processing using SIMD processor. The number of processors can be increased by connecting IMAP LSIs in series. Figure 2 shows an example of a real-time vision system with 512×512 pixel images. Using four of the IMAPs shown in Fig.1, the system contains 512 processors, each of which carries out image processing to an individual column of images.

Since the publication of that study, the authors have developed an IMAP prototype LSI which integrates eight 8 bit processors and a 144 Kbit SRAM, and a Real-Time Vision System (RVS), which uses 64 IMAP prototype LSIs. The purpose of this development has been to investigate IMAP potential, to test sequencer designs, to develop software tools and to develop image processing algorithms.

This paper describes the IMAP prototype LSI and the RVS, and it discusses the the results of its performance in image processing and in neural network simulation on the RVS.

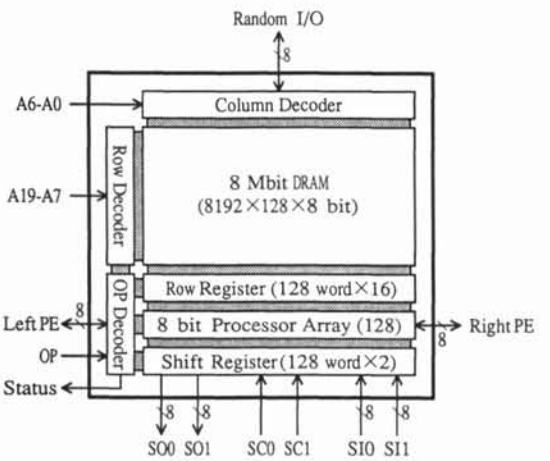


Figure 1 Integrated Memory Array Processor (IMAP)

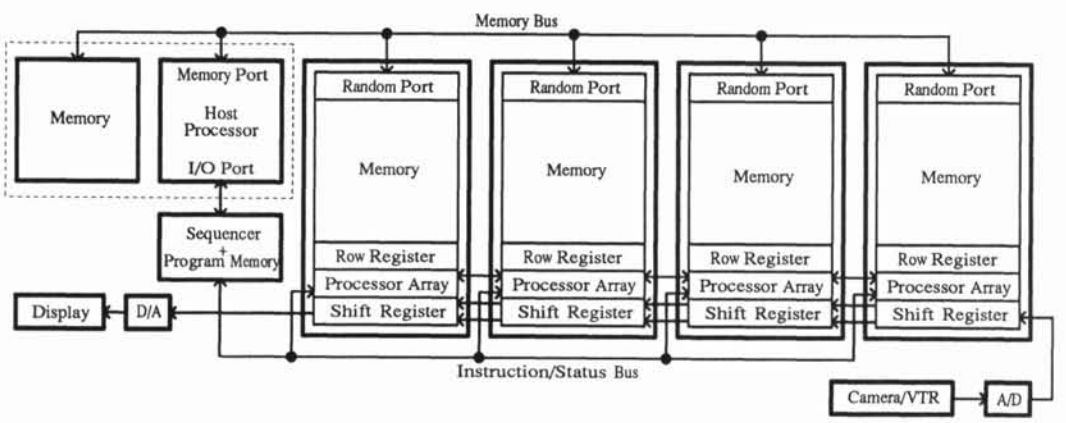


Figure 2 Real-Time Vision System Configuration

IMAP PROTOTYPE LSI

Unlike the authors' previously reported IMAP, the IMAP prototype LSI is designed so that each processor has its own separate, individual memory (rather than sharing a single large capacity memory). While this architecture does limit the number of processors which can be integrated on a single chip, the IMAP prototype LSI performs the same functions as the IMAP. As a semi-custom LSI, it is easier to fabricate.

Figure 3 shows the IMAP prototype LSI configuration. Eight SIMD processors are connected in a line, and both sides are fitted with pins for connection to additional processors. Each processor consists of a 2K byte memory, a 256 byte indirect access memory, two shift registers, an inter-processor register, a mask register, 16 byte registers, an ALU, and a shifter.

All processors individually access simultaneously the same corresponding addresses simultaneously on each of their separate memories, but addresses accessed in the indirect accesses memory may be different. Two shift registers are used for image input and output. They have the same function as the serial access memory for a VRAM [5][6]. The inter-processor register is used to transfer data between adjacent processors. With it, data stored on another processor can be accessed. The mask register maintains information as to whether or not a processor is currently active. Instructions are broadcast to all processors through an instruction bus. The logical OR value for of all status registers in each processor, which are set according to results of instructions, are sent out of the LSI. All memories are connected with a memory bus. They are directly accessible from the outside by an external processor.

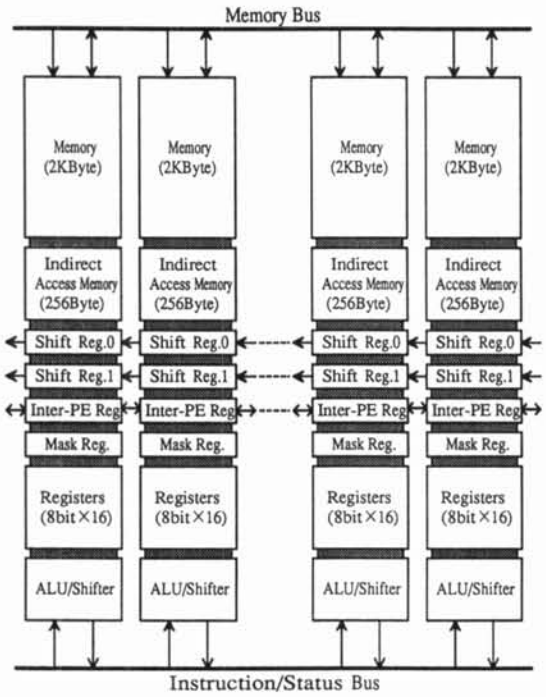


Figure 3 IMAP Prototype LSI Configuration

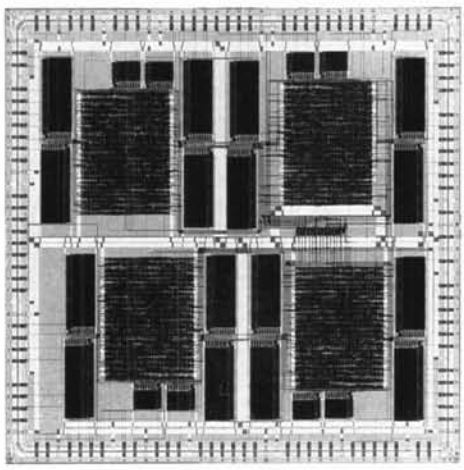


Figure 4 IMAP Prototype LSI

Figure 4 shows the chip layout for the IMAP prototype LSI. Two processors are contained on one macro block. Specifications for the IMAP prototype LSI are shown in Table 1. There are 1,112,724 transistors in the LSI. Peak performance is 200 MIPS for 8 bit operations, when used at 25 MHz.

REAL-TIME VISION SYSTEM

The authors have developed a 512 processor Real-Time Vision System (RVS) using 64 IMAP prototype LSIs. The RVS has the same configuration as shown in Fig.2, except that individual IMAPs in Fig.2 have been replaced with 16 IMAP prototype LSIs. Since each processor in the IMAP prototype LSI has a 2K byte memory, a total of four 512×512 pixel images can be held in the 64 IMAP prototype LSIs. Figure 5 shows RVS. Four processor boards, three boards for a controller and one video board plus a host workstation, are installed along a VME bus. A video camera and a monitor display are used for image data input and result output. The other display is a console for the host workstation.

Processor Board: Figure 6 shows a processor board with 16 LSIs, i.e. 128 processors. The sixteen LSIs are connected in series, in the same way as shown in Fig.2. Since the memory interface for each LSI is connected to the VME bus, an external processor on the VME bus can access memories on the IMAP prototype LSIs. The logical OR value for all status outputs from individual LSIs are sent out of the processor board. When used at 25 MHz, the processor board performance is 3.2 GIPS for 8 bit operations.

Controller Boards: The controller is comprised of the three controller boards. These boards consists of a program memory, a sequencer and a memory arbiter. A program is first loaded into the program memory from the host workstation. From there, it is sent by the sequencer to the proces-

Table 1 IMAP Prototype LSI Specifications

Processor Number	8
Total Memory Capacity	147456 bit
Memory Capacity per Processor	2304 byte
Total Transistors	1,112,724
Transistors for Memory	975,736
Transistors for Logic	136,988
Clock	25 MHz
Peak Performance	200 MIPS (8 bit)
Chip Size	14.8 mm×14.8 mm
Package	132 pin PGA

sors. The memory arbiter avoids a memory access collision at the memories on the IMAP prototype LSIs. The memory arbiter interlocks instruction issue from the sequencer to the processors, when a load/store operation is fetched at the sequencer during a memory access from the host workstation. Instructions, which are not load/store, are never interlocked and are issued concurrently with a memory access from the host workstation. Using this mechanism, the host processor and a program for IMAP prototype LSIs do not need to care about memory access collision.

Video Board: To synchronize video image input/output and image processing, horizontal and vertical synchronization signals for the video images are sent to the controller and used as interrupts to the sequencer. Thus, program initiations in every line, every field and every frame are easily controlled by using the software as an interrupt program. Data transfer between shift registers and a memory is also realized by the interrupt and is initiated by the horizontal synchronization signal.

Software: A macro assembler, a RVS simulator, a debugger and C libraries were developed as software tools. The software runs on remote workstations as well as on the host workstation.

PERFORMANCE

Several image processing algorithms have been implemented on the RVS. Their performance is shown in Table 2. All algorithms are applied to 512×512 pixel, 8 bit images. Since the controller is designed to operate at 15 MHz, image processing performance is also obtained at 15 MHz. The RVS peak performance at this clock is 7.7 GIPS.

Data parallel type algorithms, such as filters, are carried out from 955 μs to 6.5 ms. They are from about 20 or 30 times faster than the video rate (33 ms per frame). The histogram is carried out in 1.3 ms. In this algorithm, first, the histogram for each column in an image is created in each processor, using indirect access memory. Then 512 histograms are merged, using inter-processor data transfer operations. The 8×8 block size Discrete Cosine Transform (DCT) for a 512×512 pixel image is accomplished in 13 ms.

Rotation, which is not well matched to the one dimensional SIMD architecture, can be accomplished using indirect memory access and inter-processor date transfer [7]. Ninety degree rotation takes 6 ms and 30 degree rotation takes 20 ms. Obtaining two projections, both in the row direction and the column direction, are carried out by a combination of projection and 90 degree rotation.

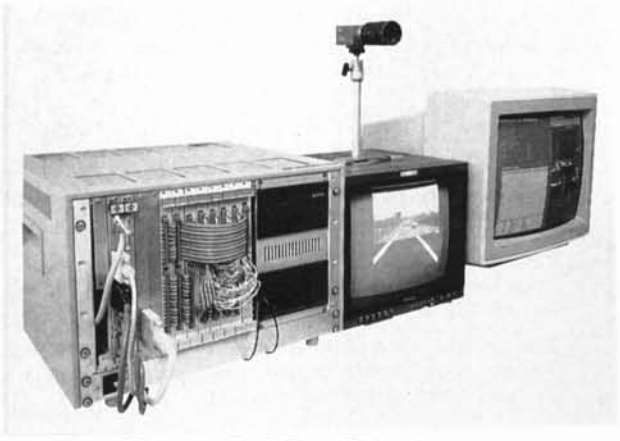


Figure 5 Real-Time Vision System

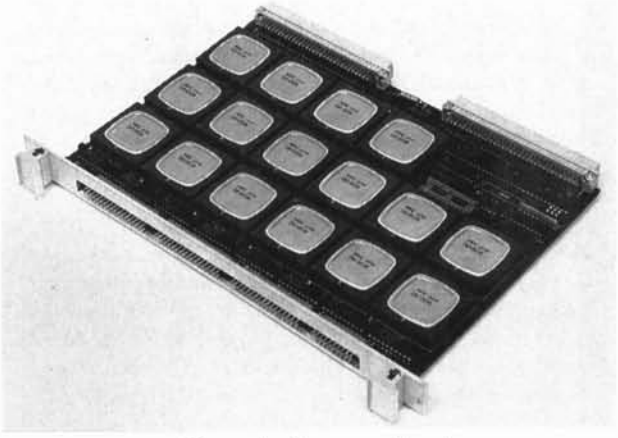
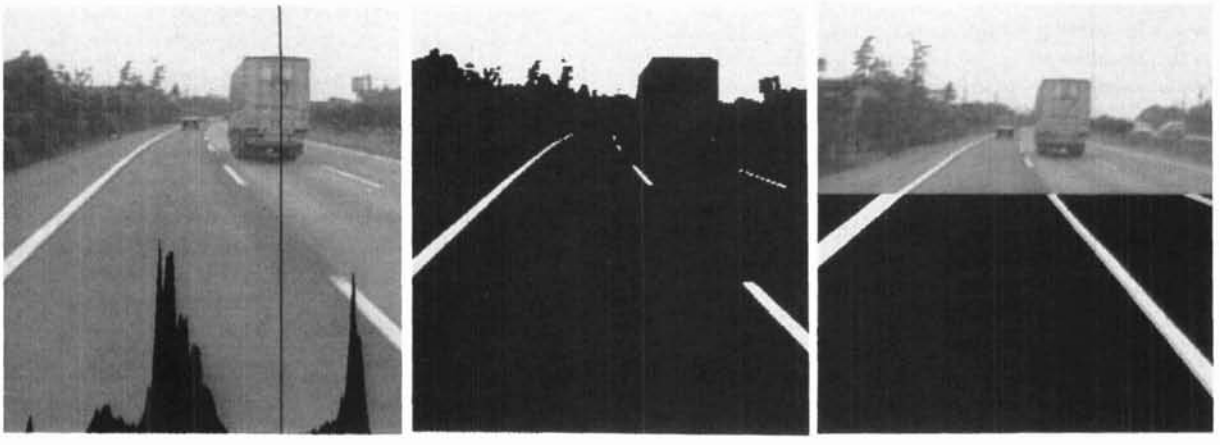


Figure 6 Processor Board

Table 2 Image Processing Performance

Algorithm	Program Lines	Object Code Length	Execution Steps	Execution Time (μs)	Ratio to Video Rate (Ratio to 33ms)
Image Subtraction	30	8	2053	137	1/244
Projection	48	32	3595	240	1/139
Averaging Filter (3×3)	118	39	14320	955	1/35
Laplacian Filter (3×3)	127	41	17417	1161	1/29
Range Filter (3×3)	115	53	23050	1537	1/22
Median Filter (3×3)	171	199	96818	6455	1/5
Thinning	566	452	74044	4936	1/7
Mozaic (16×16)	65	261	8228	549	1/61
Mozaic (8×8)	68	135	8338	556	1/60
Histogram	197	154	19877	1325	1/25
Histogram Equalization	222	126	20529	1367	1/24
DCT (8×8)	523	631	197972	13198	1/2.5
DCT + Quantization (8×8)	619	772	259106	17274	1/1.9
Rotation (90 degree)	508	368	95230	6349	1/5.3
Rotation (30 degree)	469	412	297377	19825	1/1.7
Adaptive Binarization	56	225	22897	1526	1/22



(a) Threshold Search (b) Adaptive Binarization (c) Line Connection

Figure 7 Road Image Processing

Figure 7 shows a real-time road image processing example. First, the histogram for an image is obtained in 1.3 ms. Then, the threshold level is searched for in 0.2 ms, as shown in Fig.7(a). Using the threshold, input image is binarized (Fig.7(b)). Finally, the logical OR image for the final several frames of binarized image is created to connect not-continuous white line (Fig.7(c)). This road image processing is accomplished in 1.5 ms, which is 22 times faster than the video rate of 33 ms. This means that only 1/22 of the processing power is used in this application and the 21/22 of processing power can be used for other algorithms, such as obstacle detection or car following.

The one dimensional processor architecture for the IMAP and the RVS is suitable for neural network simulation [8]–[10]. The RVS shows 197 MCPS peak performance, when the output layer neuron number is a multiple of processor number of 512. In this algorithm, input data for the neural network are broadcast to all processors, one by one. When a processor receives the input data, each processor multiplies it with a corresponding weight data stored in a memory.

The IMAP and the RVS have a big advantages, since they can hold the entire weight matrix data on the chip. For example, the RVS can simulate a network with 1064 input layer neurons, 512 intermediate layer neurons, and 512 output layer neurons.

CONCLUSION

An IMAP prototype LSI, a Real-Time Vision System (RVS) and its performance have been presented. The RVS has shown high performance, not only for a data parallel type algorithm, such as filtering and DCT, but also to a rotation of images, which is not suitable for SIMD processing.

This work confirmed that the IMAP architecture has big advantages for realizing a high performance, yet compact, real-time vision system. By developing an IMAP, shown in Fig.1, the entire real-time vision system can be integrated in one board. It can easily be incorporated in individual workstations and vision systems. The IMAP also has a big potential for use as a neuro chip.

A real-time road image processing experiment was implemented on the RVS. The white line on the road was detected and connected in 1.5 ms.

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